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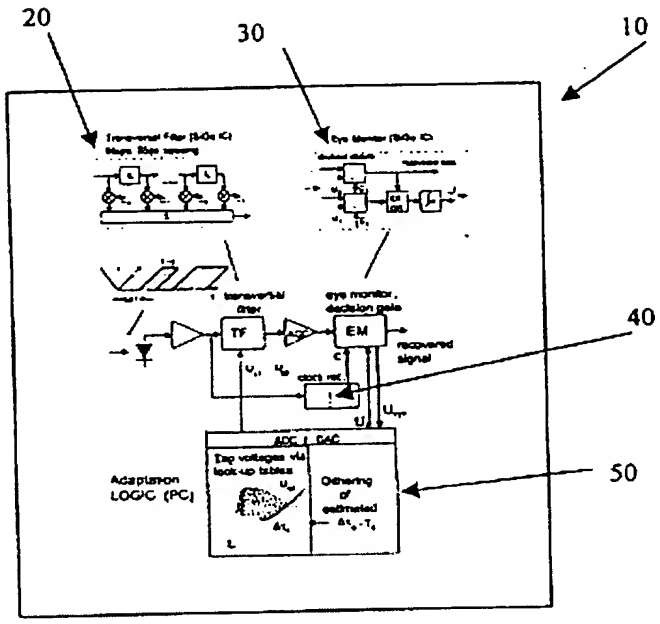


FIG. 1 (Prior Art)

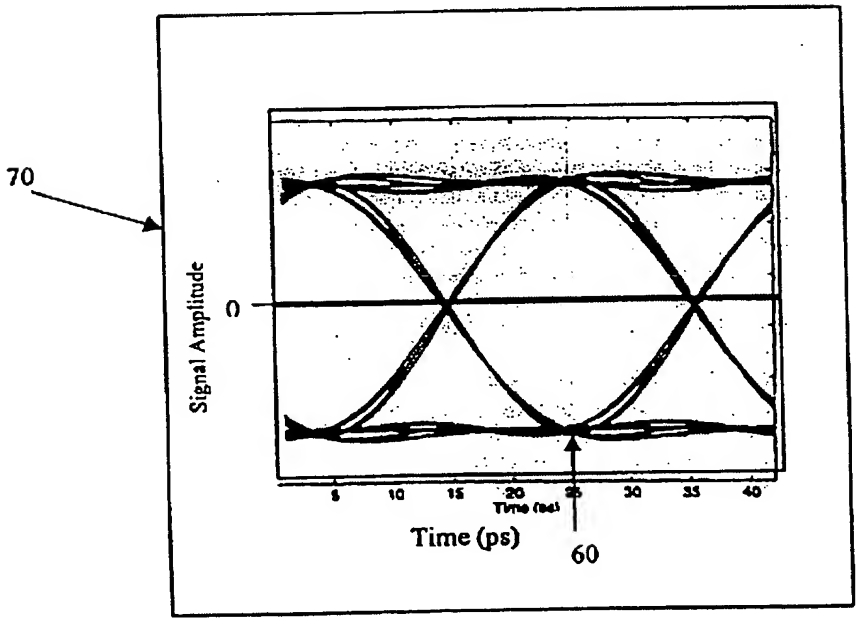


FIG. 2a (Prior Art)

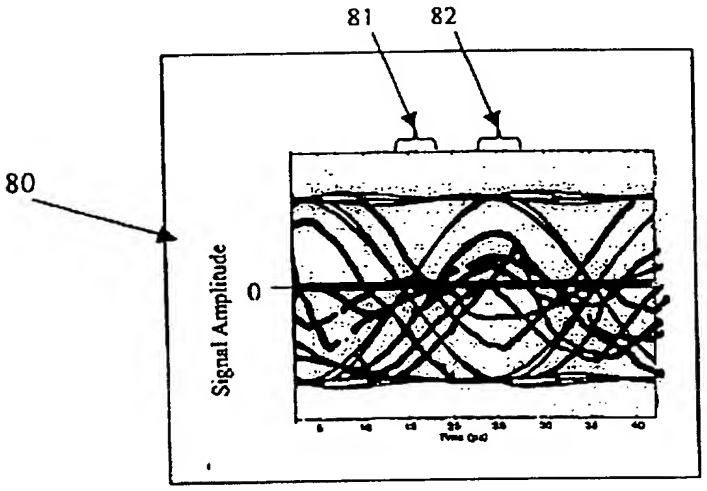


FIG. 2b (Prior Art)

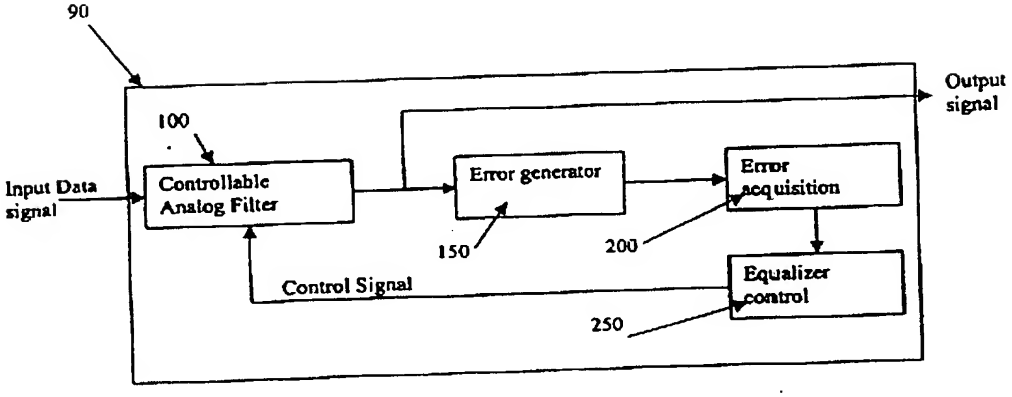


FIG. 3

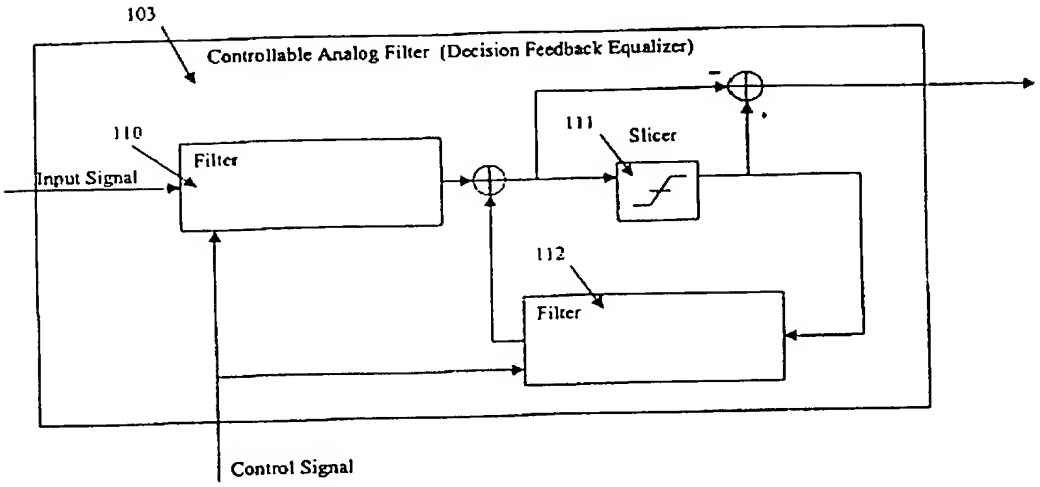

103
Controllable Analog Filter (Decision Feedback Equalizer)
110
Filter
Input Signal
111
Slicer
112
Filter
Control Signal

FIG. 4

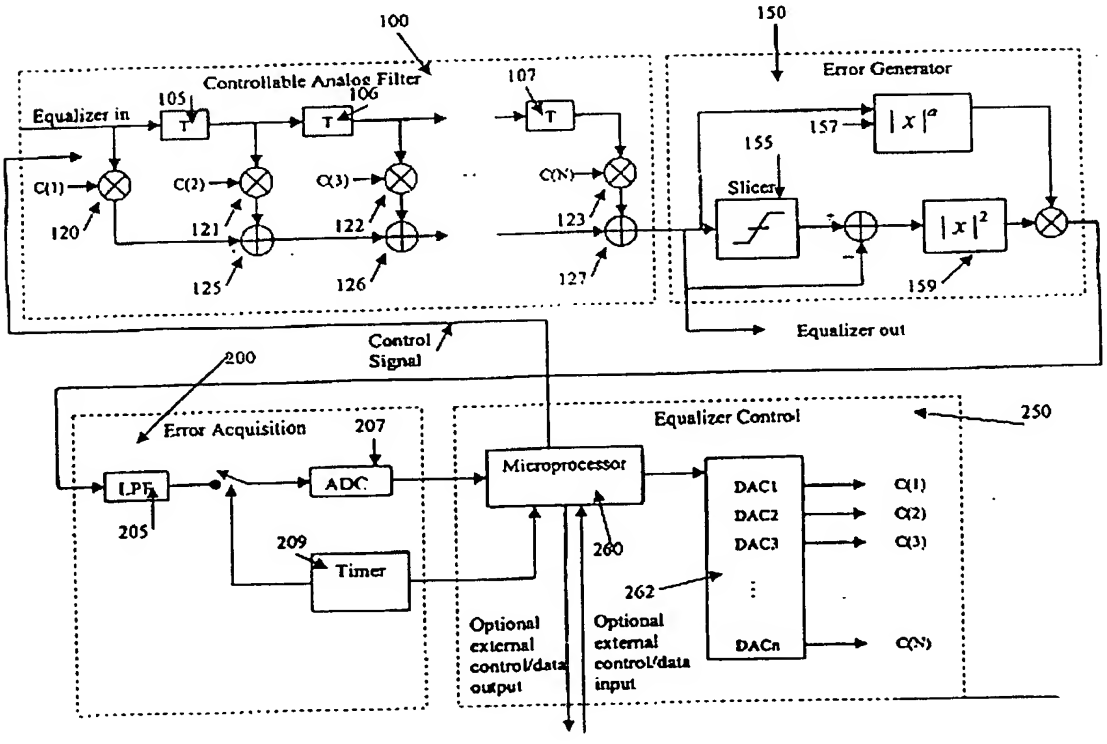

100
Controllable Analog Filter
Equalizer in
105
106
107
T
C(1)
C(2)
C(3)
C(N)
120
121
122
123
125
126
127
150
Error Generator
157
155
Slicer
159
Equalizer out
Control Signal
200
Error Acquisition
207
LPF
ADC
205
209
Timer
Equalizer Control
250
Microprocessor
260
262
DAC1
DAC2
DAC3
DACn
Optional external control/data output
Optional external control/data input

FIG. 5

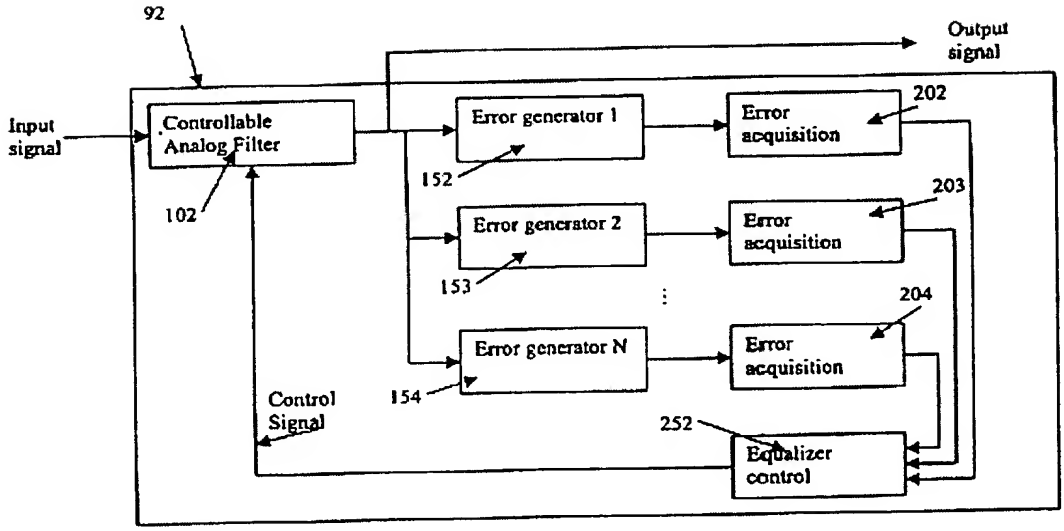

92
Output signal
Input signal
Controllable Analog Filter
102
Error generator 1
152
Error acquisition
202
Error generator 2
153
Error acquisition
203
Error generator N
154
Error acquisition
204
Control Signal
252
Equalizer control

FIG. 6

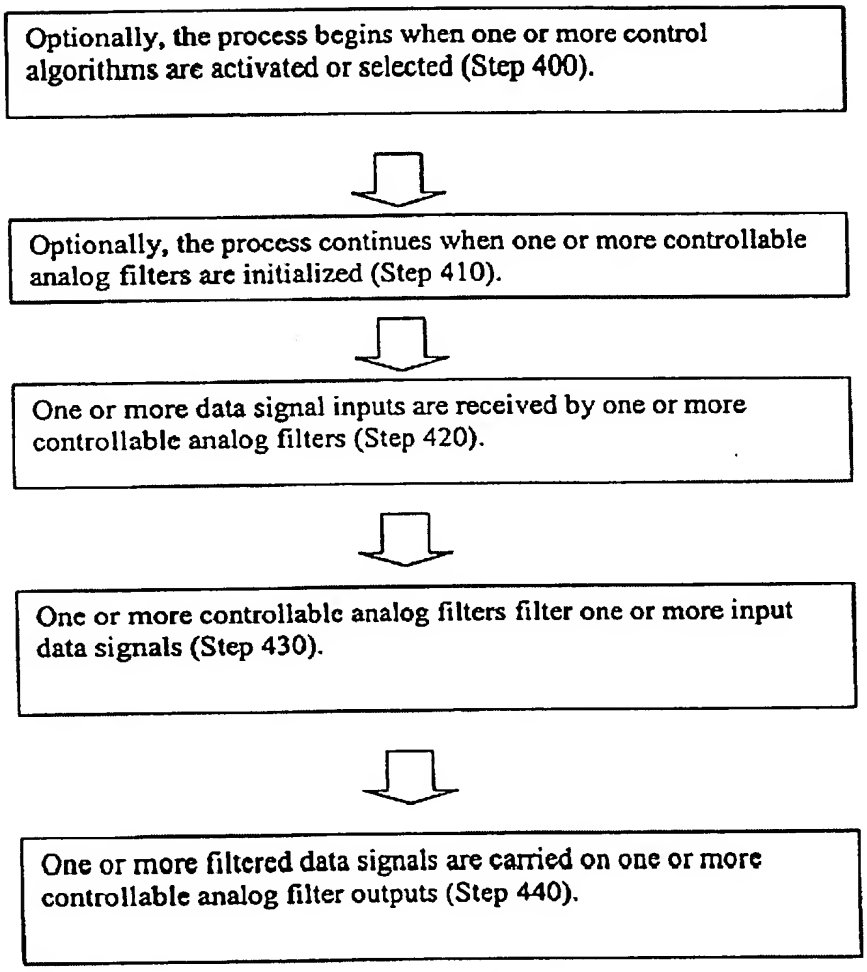

Optionally, the process begins when one or more control algorithms are activated or selected (Step 400).
Optionally, the process continues when one or more controllable analog filters are initialized (Step 410).
One or more data signal inputs are received by one or more controllable analog filters (Step 420).
One or more controllable analog filters filter one or more input data signals (Step 430).
One or more filtered data signals are carried on one or more controllable analog filter outputs (Step 440).

FIG. 7a

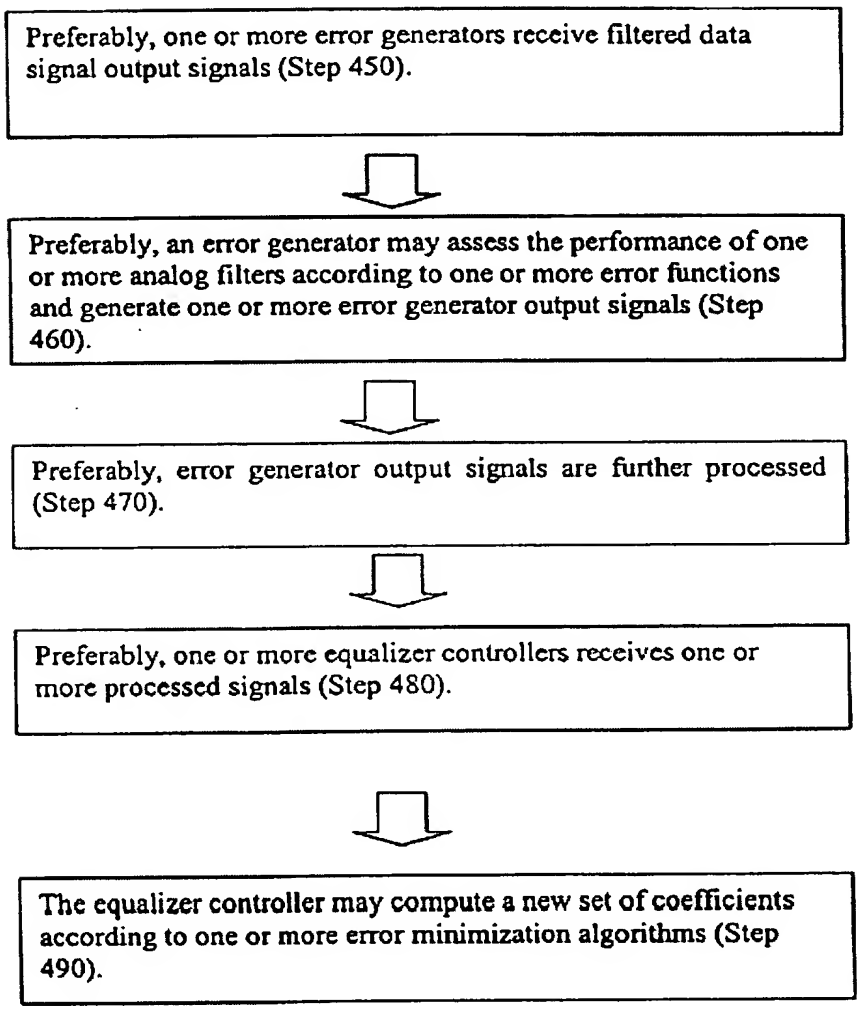

Preferably, one or more error generators receive filtered data signal output signals (Step 450).
Preferably, an error generator may assess the performance of one or more analog filters according to one or more error functions and generate one or more error generator output signals (Step 460).
Preferably, error generator output signals are further processed (Step 470).
Preferably, one or more equalizer controllers receives one or more processed signals (Step 480).
The equalizer controller may compute a new set of coefficients according to one or more error minimization algorithms (Step 490).

FIG. 7b

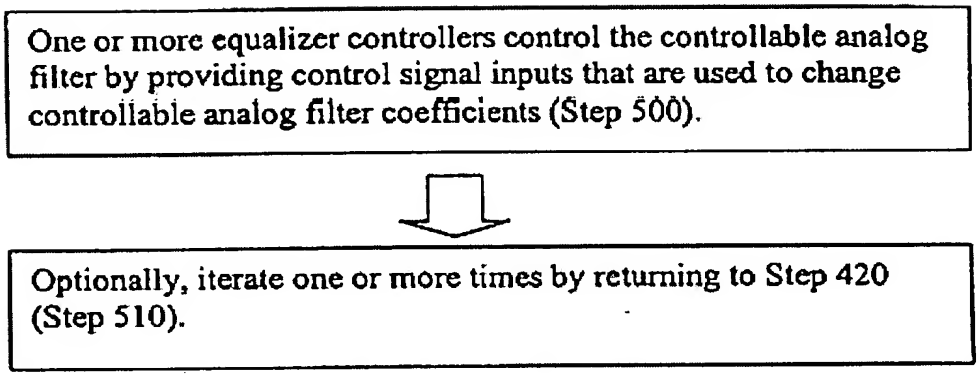

One or more equalizer controllers control the controllable analog filter by providing control signal inputs that are used to change controllable analog filter coefficients (Step 500).
Optionally, iterate one or more times by returning to Step 420 (Step 510).

FIG. 7c

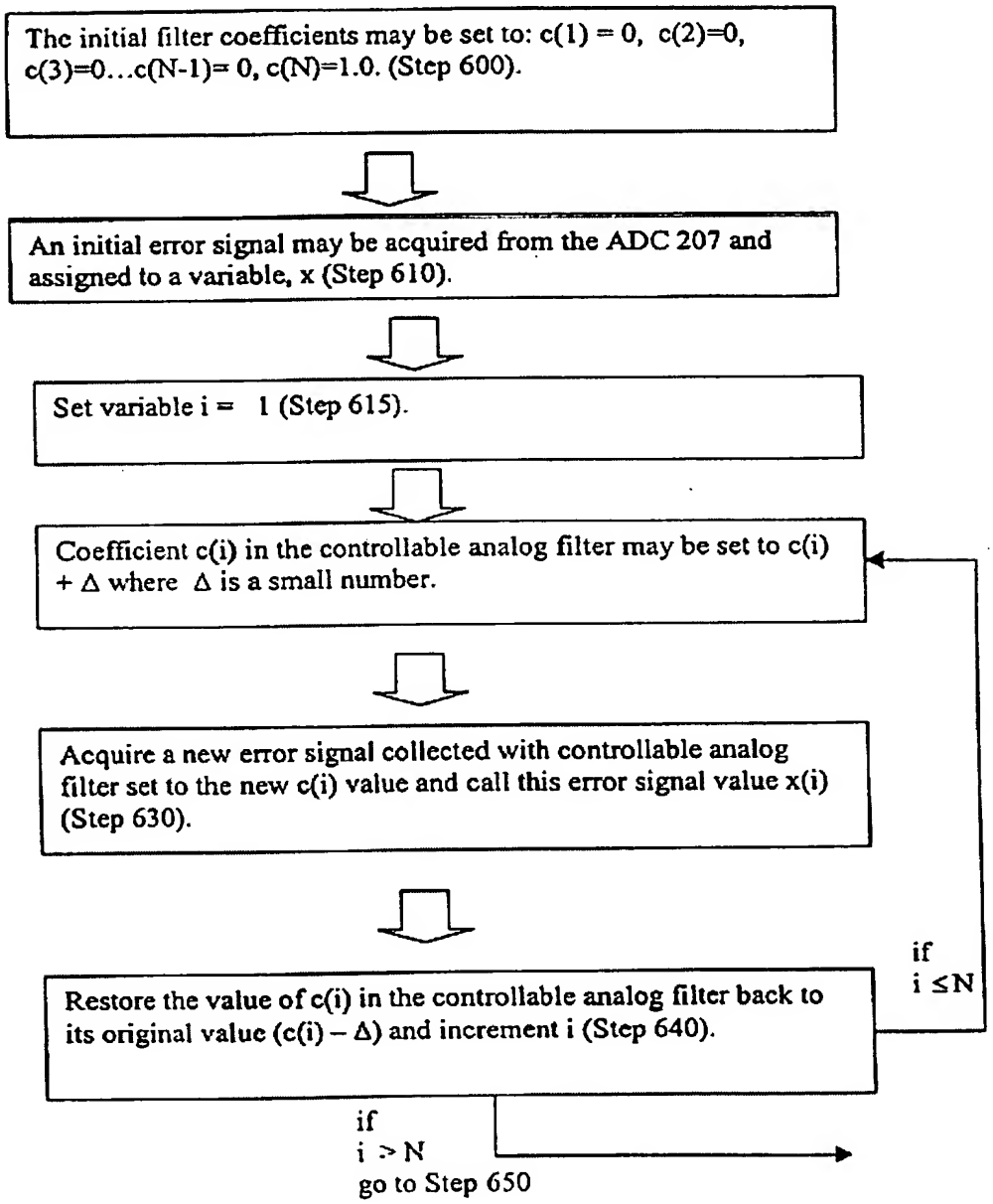

The initial filter coefficients may be set to: c(1) = 0, c(2)=0, c(3)=0...c(N-1)= 0, c(N)=1.0. (Step 600).
An initial error signal may be acquired from the ADC 207 and assigned to a variable, x (Step 610).
Set variable i = 1 (Step 615).
Coefficient c(i) in the controllable analog filter may be set to c(i) + Δ where Δ is a small number.
Acquire a new error signal collected with controllable analog filter set to the new c(i) value and call this error signal value x(i) (Step 630).
Restore the value of c(i) in the controllable analog filter back to its original value (c(i) – Δ) and increment i (Step 640).
if i ≤N
if i > N go to Step 650

FIG. 8a

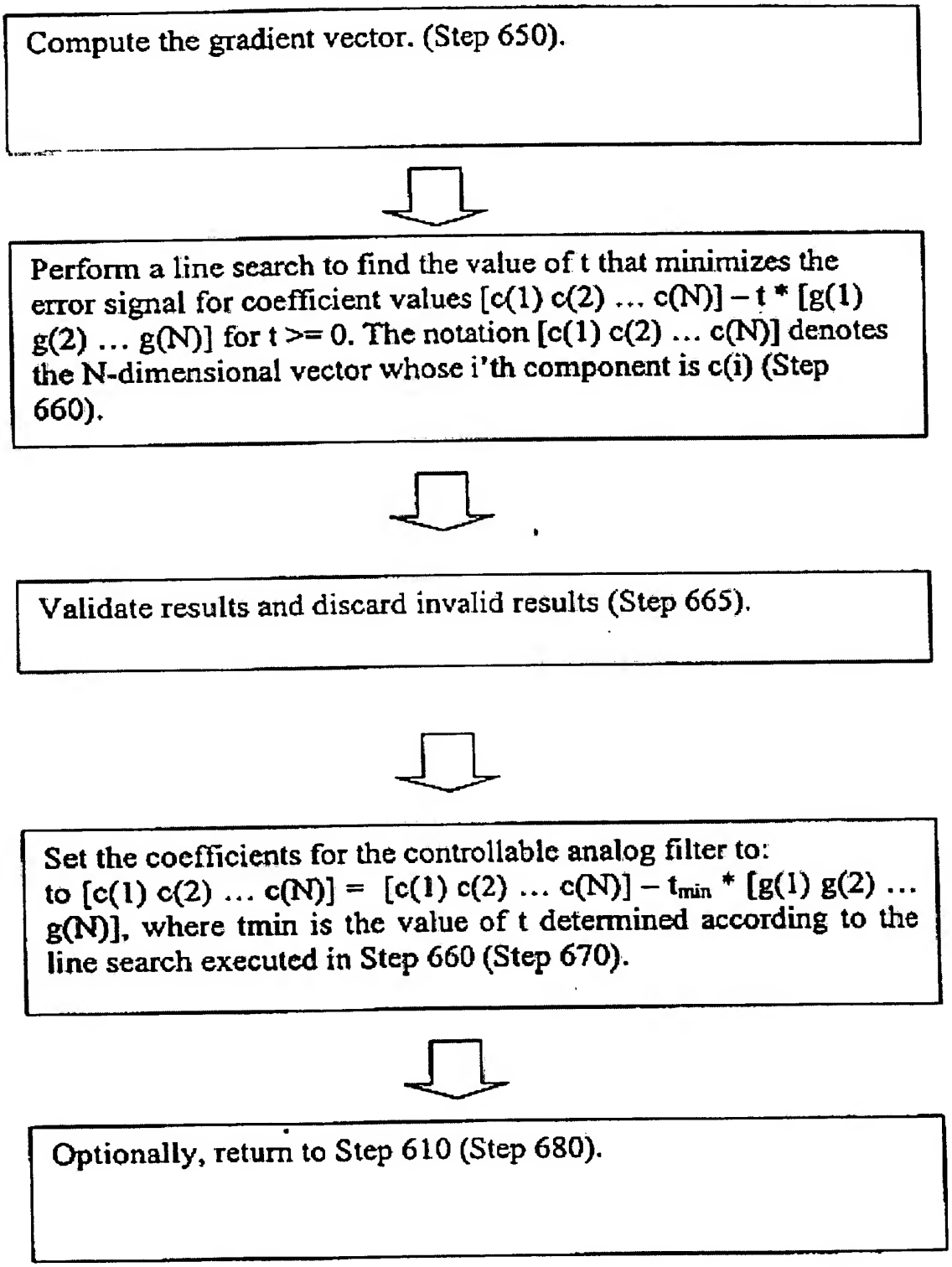

Compute the gradient vector. (Step 650).
Perform a line search to find the value of t that minimizes the error signal for coefficient values [c(1) c(2) ... c(N)] – t * [g(1) g(2) ... g(N)] for t >= 0. The notation [c(1) c(2) ... c(N)] denotes the N-dimensional vector whose i'th component is c(i) (Step 660).
Validate results and discard invalid results (Step 665).
Set the coefficients for the controllable analog filter to: to [c(1) c(2) ... c(N)] = [c(1) c(2) ... c(N)] – t_{min} * [g(1) g(2) ... g(N)], where tmin is the value of t determined according to the line search executed in Step 660 (Step 670).
Optionally, return to Step 610 (Step 680).

FIG. 8b

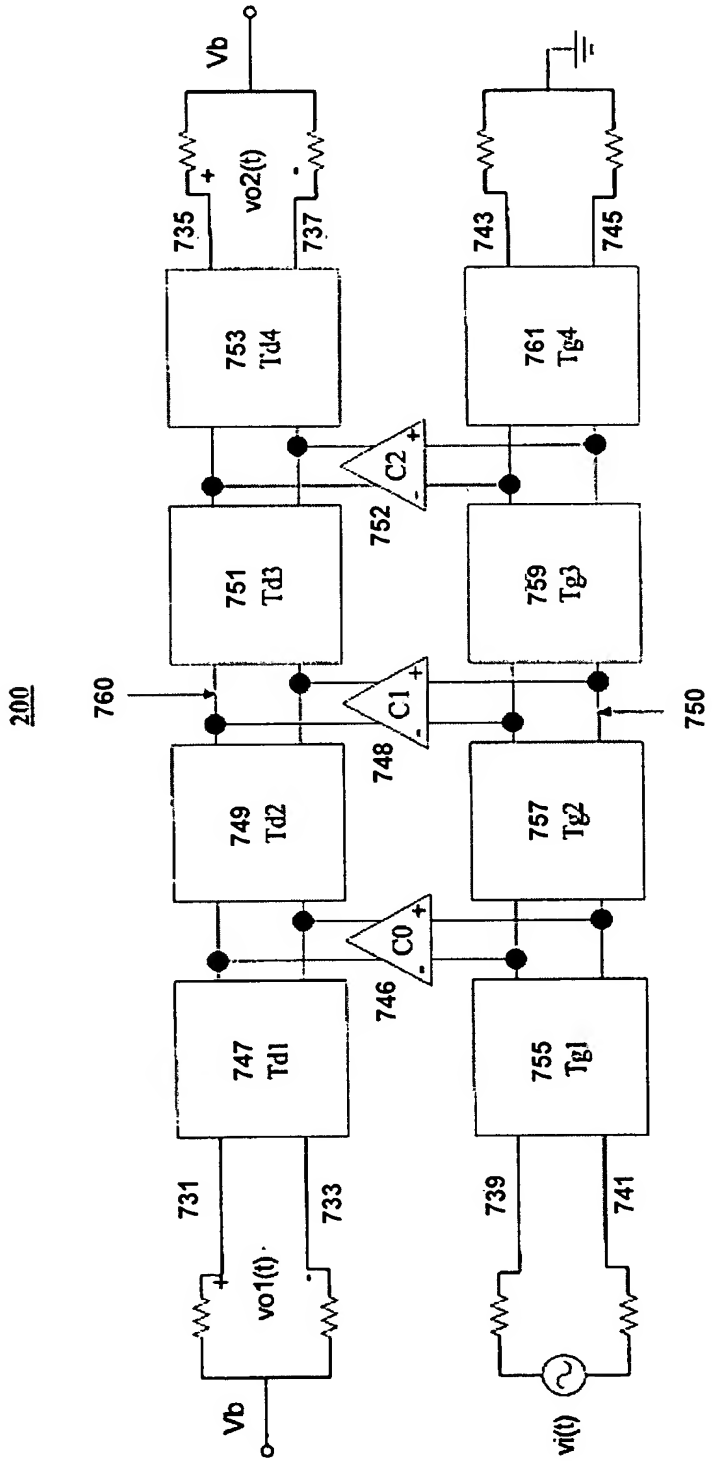

200
Vb
vo2(t)
735
737
743
745
753
Td4
761
Tg4
C2
752
751
Td3
759
Tg3
760
C1
748
750
749
Td2
757
Tg2
C0
746
747
Td1
755
Tg1
731
733
739
741
vo1(t)
Vb
vi(t)

FIG. 9

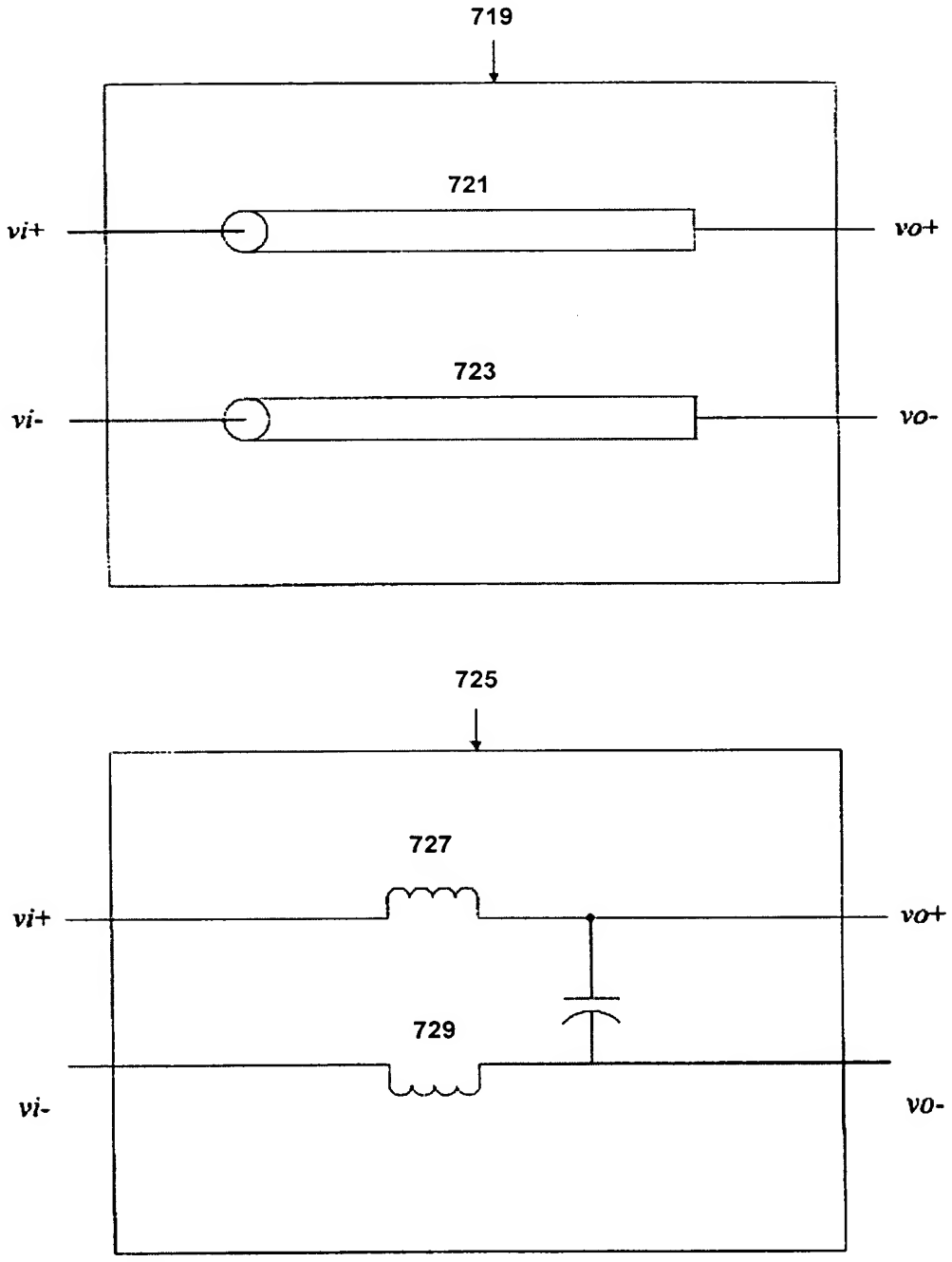


FIG. 10

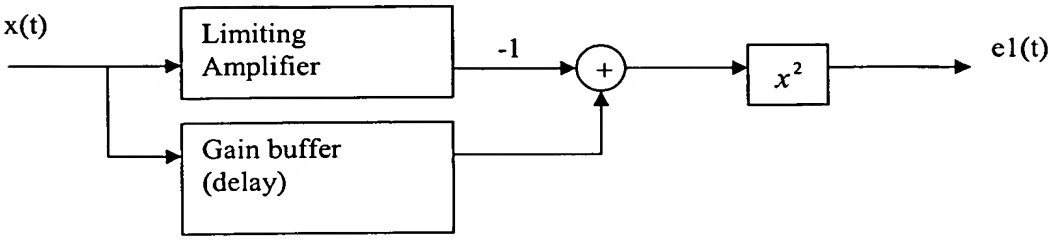
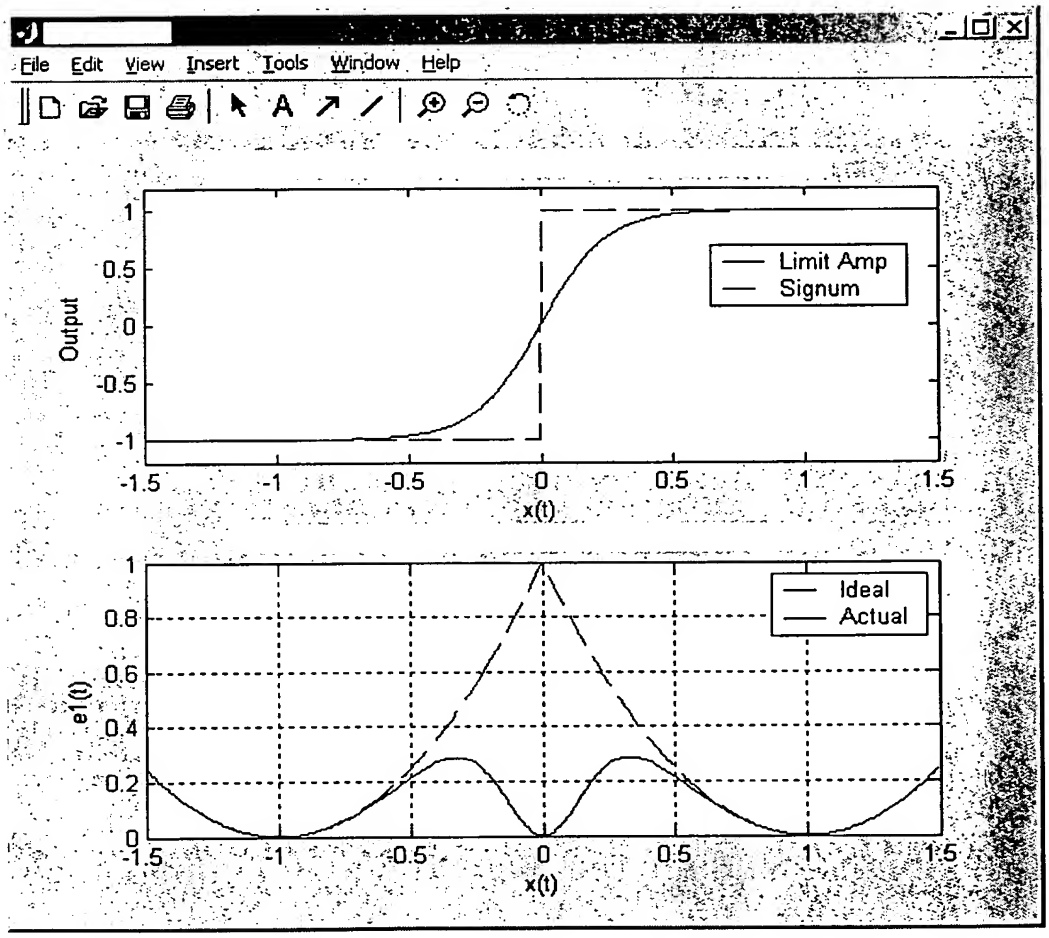


FIG. 11

FIG. 12a

FIG. 12b



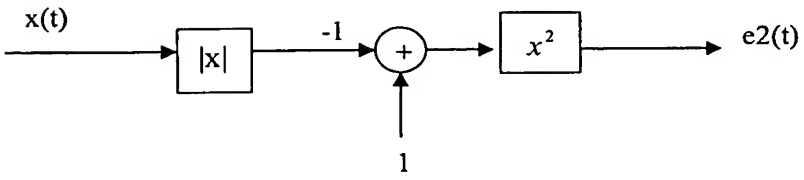


FIG. 13a

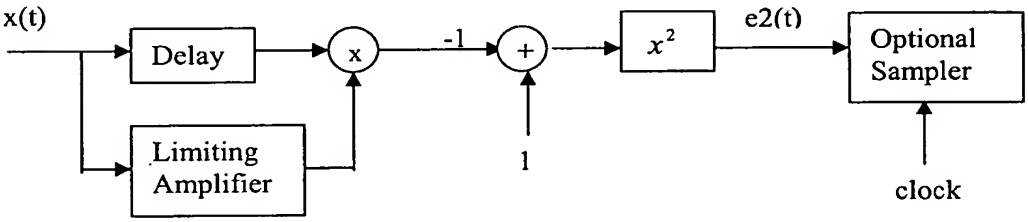


FIG. 13b

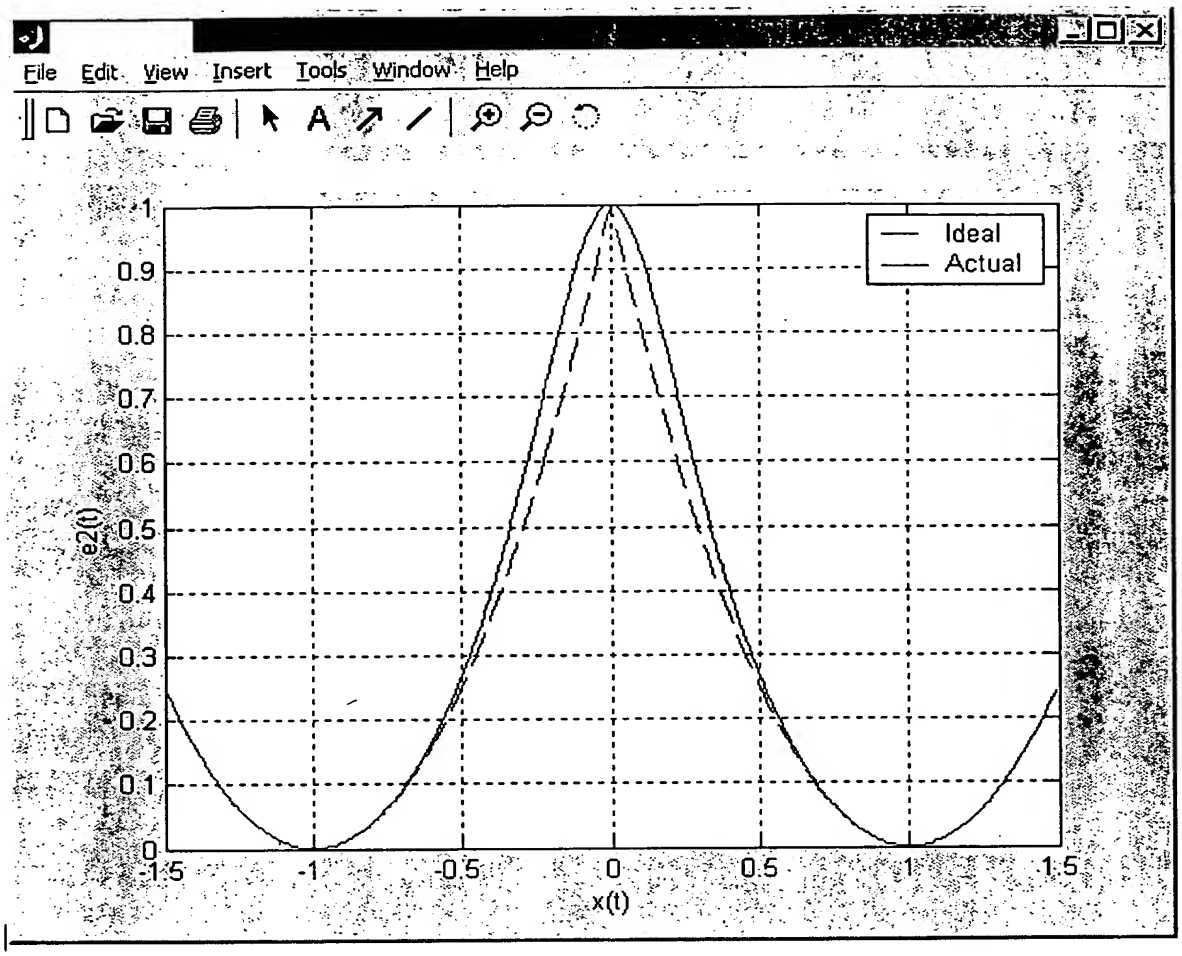

File Edit View Insert Tools Window Help
Ideal
Actual
e2(t)
x(t)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1.5
-1
-0.5
0
0.5
1
1.5

FIG. 14

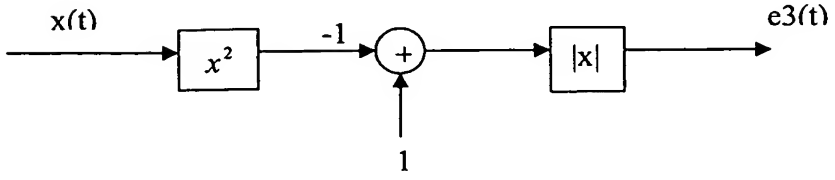


FIG. 15

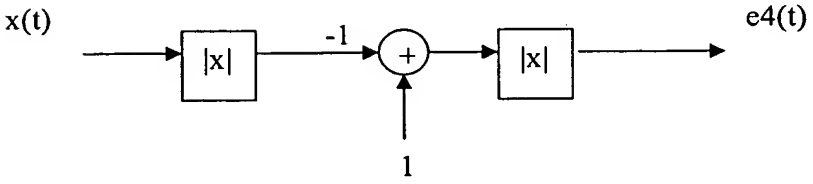


FIG. 16

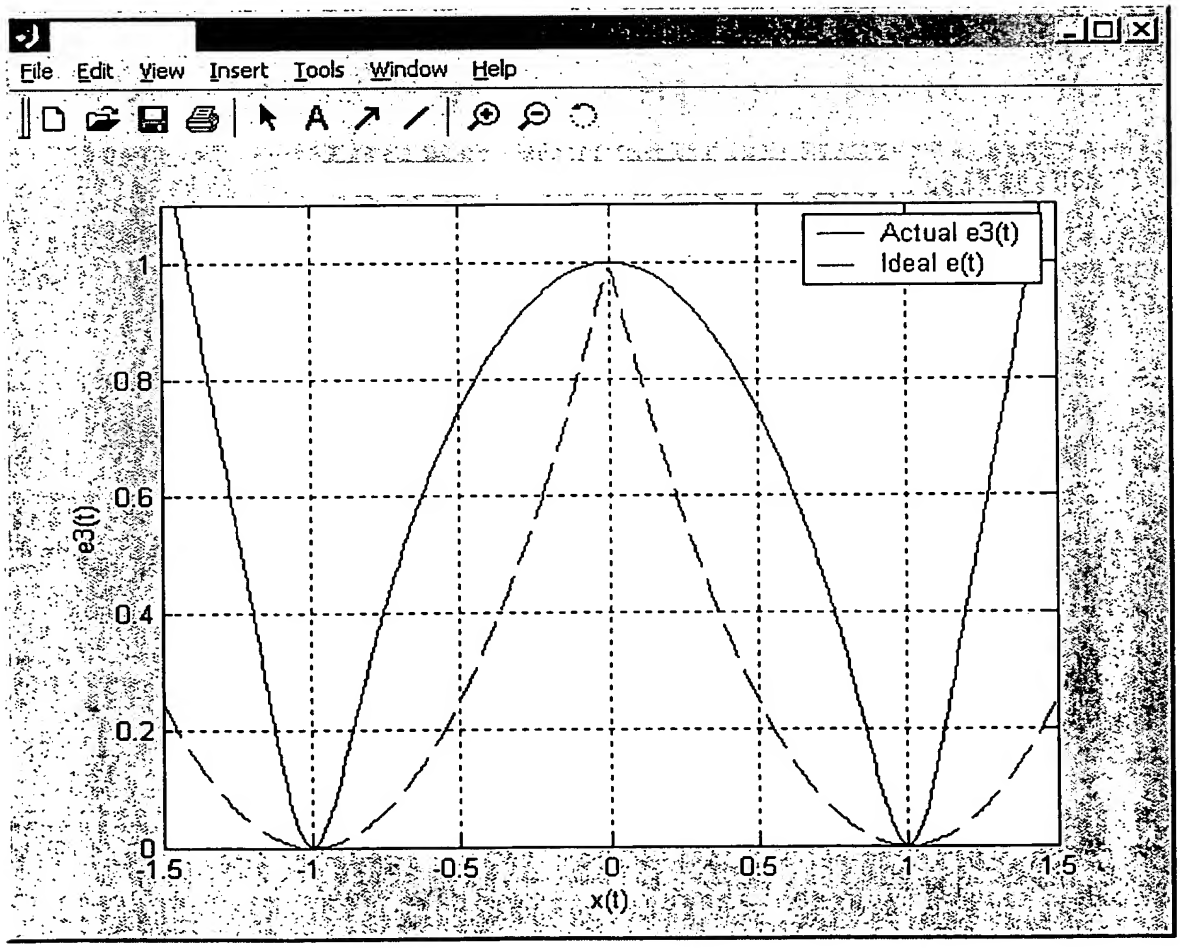


FIG. 17

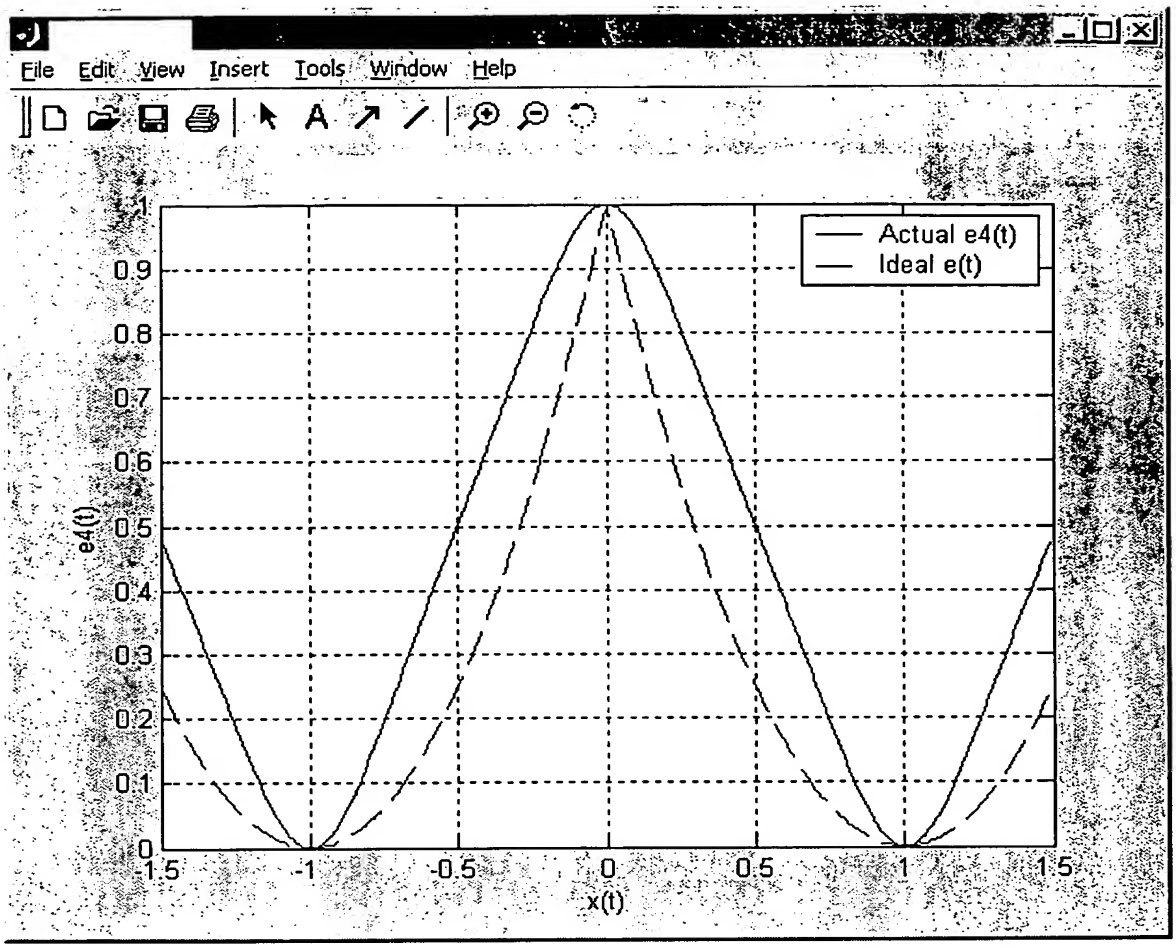

File Edit View Insert Tools Window Help
Actual e4(t)
Ideal e(t)
e4(t)
x(t)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-1.5
-1
-0.5
0
0.5
1
1.5

FIG. 18

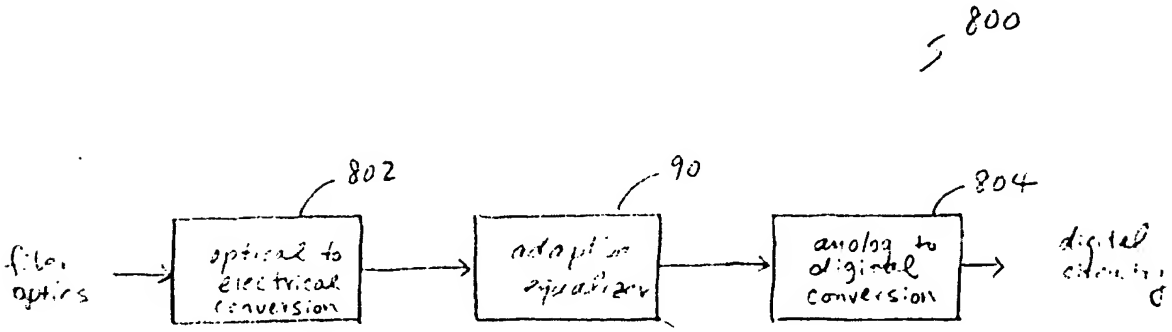

800
802
90
804
optical to electrical conversion
analog to digital conversion

FIG. 19

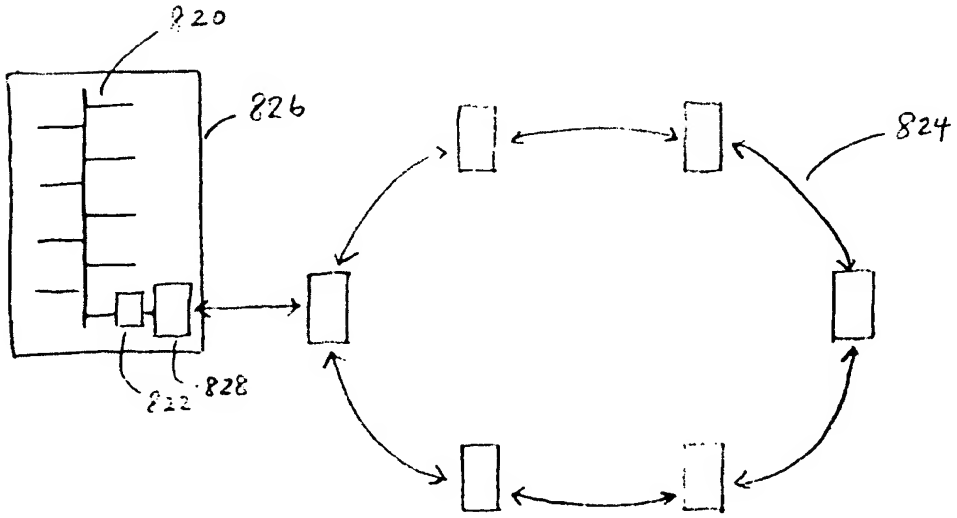

820
826
824
822
828

FIG. 20

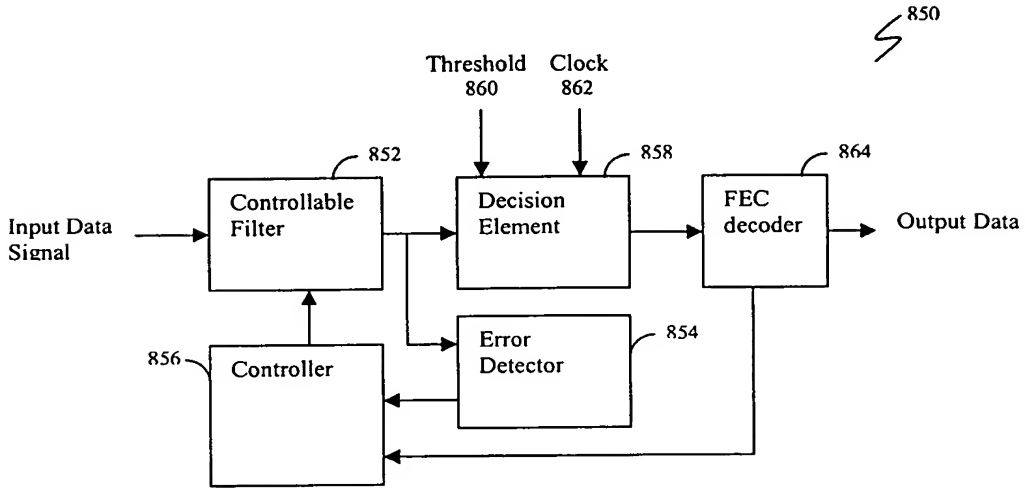

850
Threshold
860
Clock
862
852
858
864
Input Data
Signal
Controllable
Filter
Decision
Element
FEC
decoder
Output Data
Error
Detector
854
856
Controller

FIG. 21

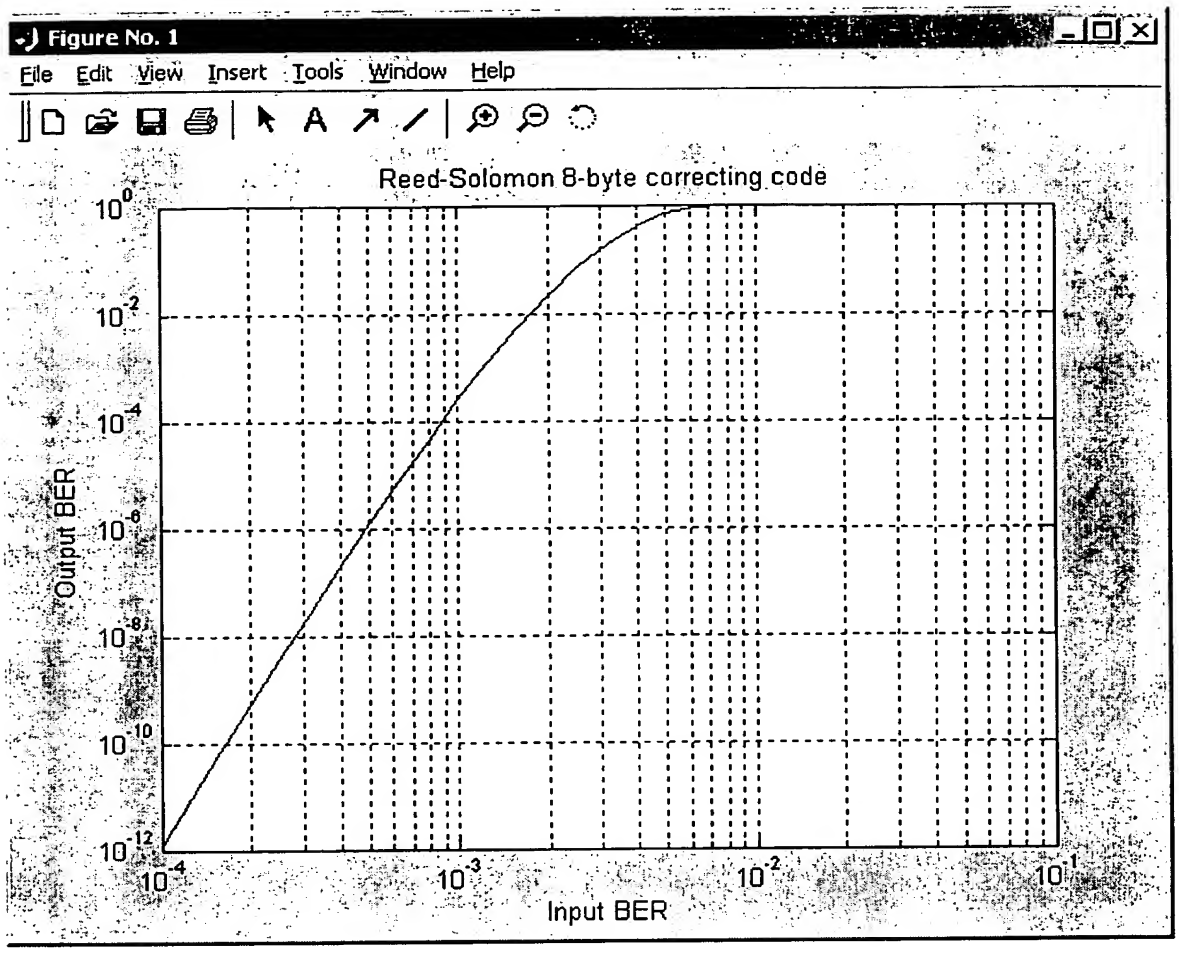


Figure No. 1
File Edit View Insert Tools Window Help
Reed-Solomon 8-byte correcting code
Output BER
Input BER
10^0
10^-2
10^-4
10^-6
10^-8
10^-10
10^-12
10^-4
10^-3
10^-2
10^-1

FIG. 22

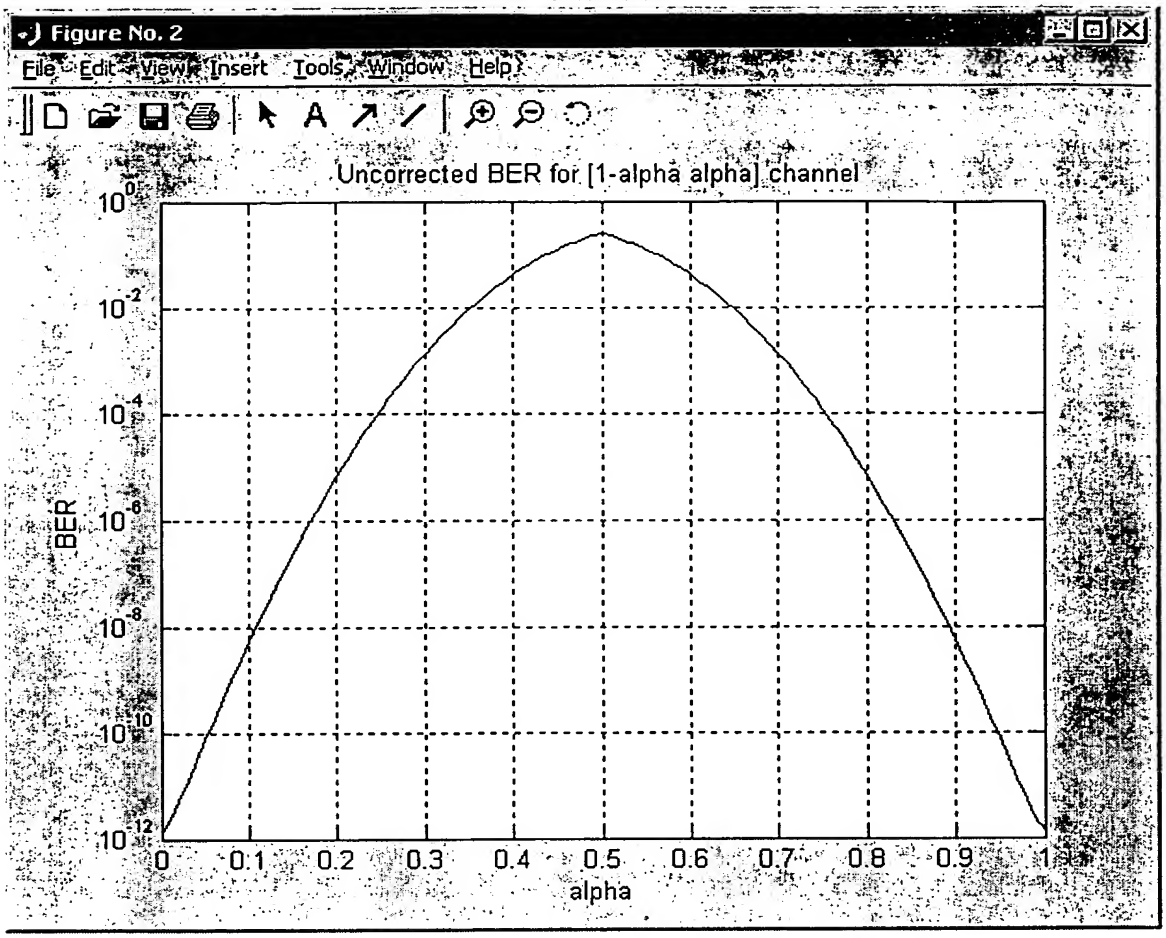


Figure No. 2
File Edit View Insert Tools Window Help
Uncorrected BER for [1-alpha alpha] channel
BER
alpha
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

FIG. 23

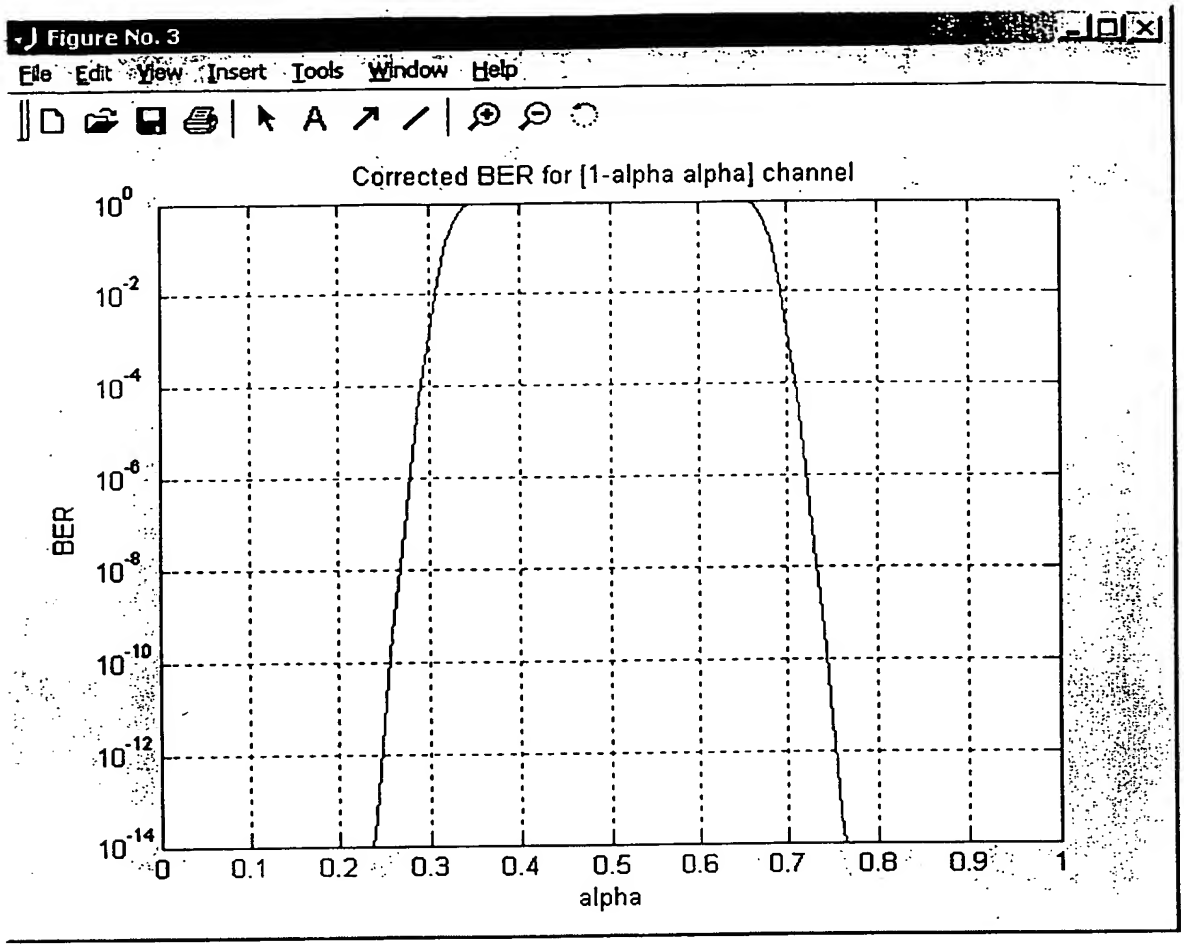


Figure No. 3
File Edit View Insert Tools Window Help
Corrected BER for [1-alpha alpha] channel
BER
alpha
10^0
10^-2
10^-4
10^-6
10^-8
10^-10
10^-12
10^-14
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

FIG. 24

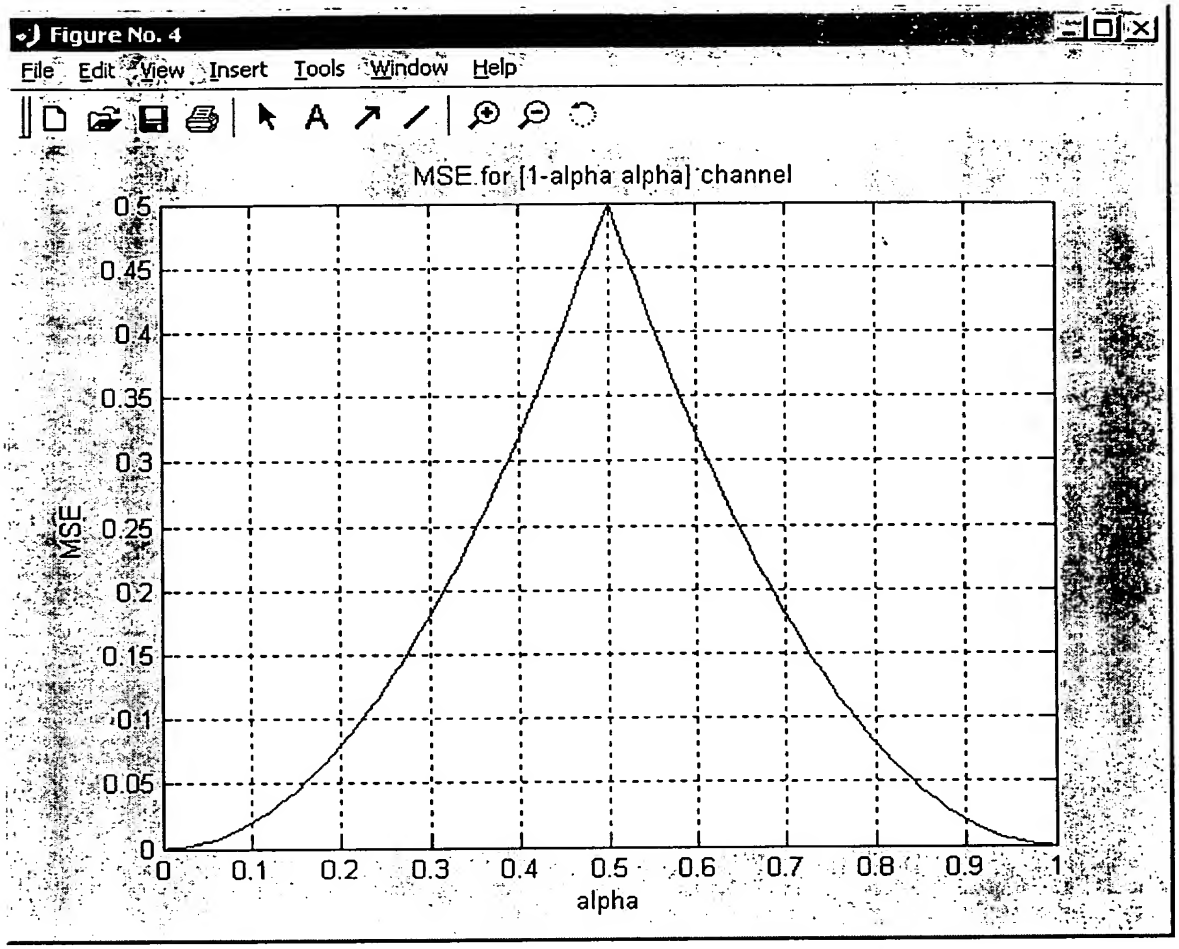


Figure No. 4
File Edit View Insert Tools Window Help
MSE for [1-alpha alpha] channel
MSE
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
alpha

FIG. 25